MORNSUN®

TD551SCANHS
SOIC 16 package isolated CAN Transceiver

Features

- Ultra-small, ultra-thin, chip scale SOIC package
- Compliant with ISO11898-2 standard
- Integrated efficient isolation power supply
- I/O power supply range supports 4.5V and 5.5V
- High isolation to 5000Vrms
- Bus-Pin ESD protection up to 8kV(HBM)
- Baud rate up to 5Mbps
- -58V to 58V bus fault protection
- High CMTI: 180 kV/μs (typical)
- TXD dominant time-out function
- Nanosecond level communication delay
- The bus supports maximum 110 nodes
- Industrial operating ambient temperature range: -40℃ to +125℃

Package



Applications

- Industrial automation, control, sensors and drive systems
- Building and greenhouse environmental control(HVAC) automation
- Security system
- Transport
- Medical treatment
- Telecommunication
- CAN Bus standard such as CAN open, Device Net, NMEA2000, ARNIC825, ISO11783, CAN Kingdom, CAN aerospace

Functional Description

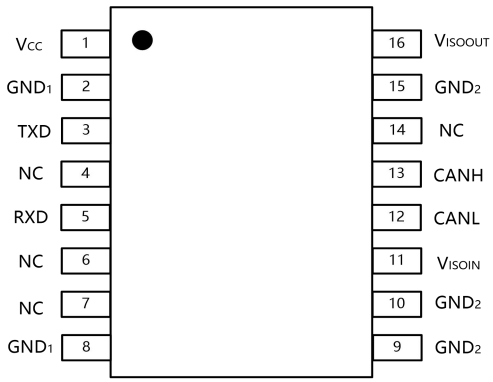
TD551SCANHS is a isolated CAN Bus transceiver, which is compliant with ISO11898-2 standard. TD551SCANHS integrate 5V quarantine power. The TD551SCANHS provide differential transmitting and receiving capability between the CAN protocol controller and the physical layer bus. It is capable of running at data of rates up to 5Mbps. The device has over-voltage(-58V to 58V) and thermal shutdown so that it is especially suitable for working in harsh environment.

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Contents

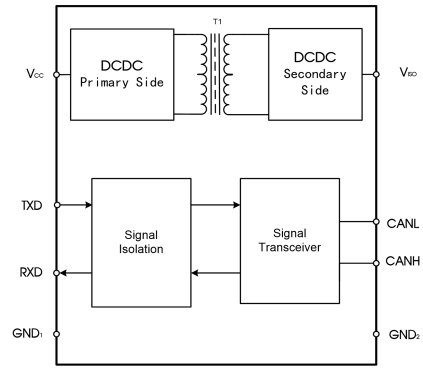
1 Home.....1
1.1 Feature and Package.....1
1.2 Applications.....1
1.3 Functional Description.....1
2 Pin Package and internal block diagram.....2
3 IC Related Parameters.....3
3.1 Absolute Maximum Rating.....3
3.2 Recommended Operating Conditions.....3
3.3 Electrical Characteristics.....4
3.4 Transmission Characteristics.....4
3.5 Physical Information.....5
4 Parameter testing circuit.....5
5 Detailed Description.....5
6 Application Circuit.....6
7 Suggestions for Power Supply.....6
8 Package Information.....7
9 Tape & Reel Information.....7

Pin Connection



Note：Pin2 and Pin8 GND1 are internally connected;
Pin15 and Pin9&10 GND2 are internally connected;

Internal Block Diagram



Function Table

Letter	Description
H	High-Level
L	Low-Level
X	Unrelated
Z	High Impedance

Table 1. Driver Function table

Input	Output		Bus State
TXD	CANH	CANL	
L	H	L	Dominant
H （Or No Connection）	Z	Z	Recessive

Table 2. Receiver Function table

V_{ID}=CANH-CANL	RXD	Bus State
V_{ID}≥0.9V	L	Dominant
0.5< V_{ID}<0.9V	Uncertainty	Uncertainty
V_{ID}≤0.5V	H	Recessive
Open	H	Recessive

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Pin Descriptions

Pin Number	Pin Name	Pin Functions
1	V_{CC}	Power supply pin. 0.1uF and 10uF ceramic capacitor must be connected to the logic side reference ground GND1 .
2	GND_1	Ground(Logic side)
3	TXD	Driver input pin
4	NC	No connect
5	RXD	Receiver output pin.
6	NC	No connect
7	NC	No connect
8	GND_1	Ground(Logic side). The pin needs to be connected to pin2 in application.
9	GND_2	Ground (Bus side). The pin needs to be connected to pin15 in application.
10	GND_2	Ground (Bus side). The pin needs to be connected to pin15 in application.
11	V_{ISOIN}	Insulation power input. The pin needs to be connected to pin16 in application.
12	CANL	CANL pin
13	CANH	CANH pin
14	NC	No connect
15	GND_2	Ground (Bus side)
16	V_{ISOOUT}	Insulation power output. 0.1uF and 10uF ceramic capacitor must be connected to the logic side reference ground GND_2. The pin needs to be connected to pin11 in application.

Absolute Maximum Ratings

General test conditions: Free-air, normal operating temperature range (unless otherwise specified).

Parameters	Unit
Supply voltage Vcc	-0.5V to +6V
Logic-side input voltage Vin	-0.5V to V_{CC}+0.5V
Bus-side voltage (CANH, CANL)	-58 to 58V
Output current I_O	-10mA to +10mA
Junction temperature T_J	< 150℃
Operating temperature range	-40°C to +125°C
Storage temperature range	-65°C to +150°C

Important: Exposure to absolute maximum rated conditions for an extended period may severely affect the device reliability, and stress levels exceeding the “Absolute Maximum Ratings” may result in permanent damage. All voltage values are based on the reference ground(GND) maximum voltage not exceeding 6V.

Recommended Operating Conditions

Parameters		Min.	Typ.	Max.	Unit
V_{CC}	Power supply	4.5	5	5.5	V
V_I or V_{IC}	Bus input pin withstand voltage (differential mode)	-30		30	V
V_{IH}	TXD High level output voltage	2		Vcc+0.3	V
V_{IL}	TXD low level output voltage	-0.3		0.8	V
T_A	Operating temperature range	-40		125	°C
T_J	Junction temperature T_J			150	°C
$T_{J(shutdown)}$	Thermal shutdown temperature		165		°C
	Signaling rate			5	Mbps

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Electrical Characteristics

General test conditions and V_{CC}=V_{ISO}= 5V, Ta = 25℃ (unless otherwise specified).

Parameters		Conditions	Min.	Typ.	Max.	Unit
Driver						
$\|V_{O(D)}\|$	Dominant CANH output voltage	Figure 1, V_{TXD} = 0 V, R_L = 60 Ω	2.75	3.5	4.5	V
	Dominant CANL output voltage		0.5		2	
$V_{O(R)}$	Recessive bus voltage	V_{TXD} = 2 V, No load	2	2.5	3	V
$V_{OD(D)}$	Differential output voltage	Figure 1, V_{TXD} = 0 V, R_L = 60Ω	1.5		3	V
$V_{OD(R)}$	Recessive differential output voltage	R_L=60 Ω	-0.05		0.05	V
I_{IH}	TXD High-level input current	V_{TXD} =2 V			20	uA
I_{IL}	TXD Low-level input current	V_{TXD} =0.8 V	-20			uA
CMTI	Common mode transient immunity	V_I = 0 or V_I =V_{CC}		180		kV/us
Receiver						
V_{IT+}	Positive-going input threshold voltage				900	mV
V_{IT-}	Negative-going input threshold voltage		500			mV
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})			120		mV
V_{OH}	High-level output voltage	Figure 2; I_{OH} = -4 mA	V_{CC} – 0.4	4.8		V
V_{OL}	Low-level output voltage	Figure 2; I_{OL} = 4 mA	0	0.2	0.4	V
R_{IN}	Input resistance (CANH or CANL)	V_{TXD} = 3 V	50		80	kΩ
Supply and Protection						
V_{ISO}	Isolated power output voltage	No load, I_{ISO}=0mA	4.8	5.06	5.3	V
I_{VCC}	Supply current(Logic side)	V_I = 0 V,R_L = 60 Ω, Access to the main dynamic protection		75	120	mA
		V_I = V_{CC}, hostage-taking		23	30	
ESD	HBM mode	CANH, CANL inter-pin to GND			±8	kV
	Contact discharge mode	CANH, CANL			±4	kV
Insulation characteristics						
V_{I-O}	Isolation voltage	Input-Output, Leakage current<1mA Rise time 3s, Fall time 1s V_{TEST}=V_{ISO}, t=60s, V_{TEST}=1.2 x V_{ISO}, t=1s(100% production test)	--	--	5000	Vrms
R_{I-O}	Insulation resistance		1			GΩ

Transmission Characteristics

General test conditions and V_{CC}=V_{ISO}= 5V, Ta = 25℃ (unless otherwise specified).

Parameters		Conditions	Min.	Typ.	Max.	Unit
t_{onTxD}	Propagation delay TXD On to bus active	Figure 3 R_L = 60 Ω, C_L = 100 pF		75	100	ns
t_{offTxD}	Propagation delay TXD Off to bus inactive			100	120	ns
t_r	Differential output signal rise time			70		ns
t_f	Differential output signal fall time			70		ns
t_{onRxD}	Propagation delay RXD On to receiver active			70	100	ns
t_{offRxD}	Propagation delay RXD Off to receiver inactive			75	140	ns
t_r	Output Signal Rise			3	6	ns
t_f	Output Fall Time			3	6	ns
T_{loop}	T_{loop} delay			120	200	ns
t_{TXD_DTO}	Dominant time-out time	C_L=100 pF	0.3		3	ms

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Physical Specifications

Parameters	Value	Unit
Weight	0.4(Typ.)	g

Test Circuits

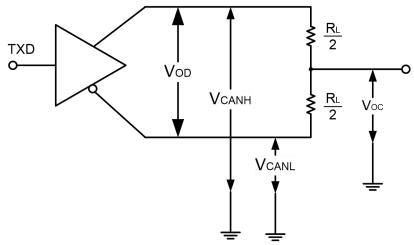


Figure 1. Driver test circuit

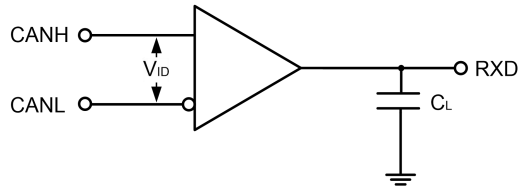


Figure 2. Receiver test circuit

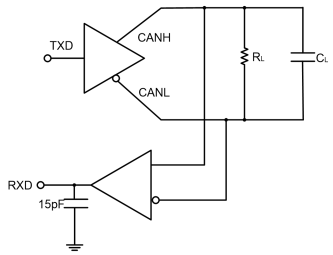


Figure 3. Switching characteristics test circuit

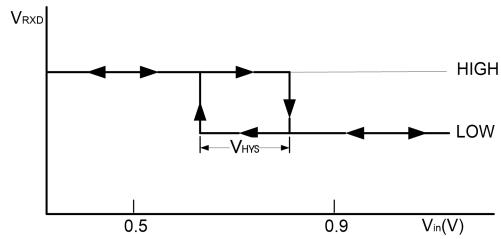


Figure 4. Receiver input hysteresis

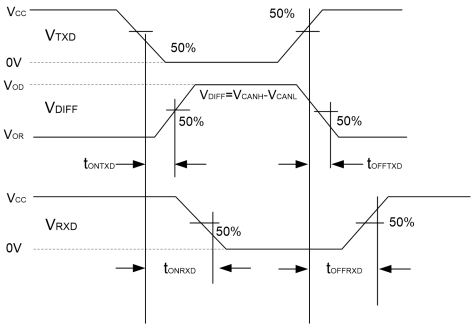


Figure 5. Drive and receiver propagation delay

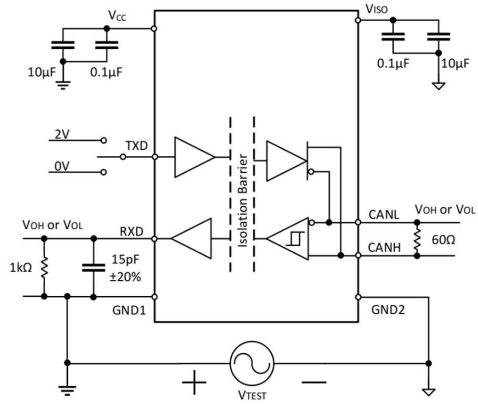


Figure 6.CMTI Test Circuit

Detailed Description

TD551SCANHS is a CAN of a style of separation transceiver with the ability of differential signal transmission between the bus and CAN protocol controller, it the inner integration insulate DC/DC power supply.which is compliant with ISO11898-2 standard.

Short-circuit protection: TD551SCANHS has current-limiting protection to prevent the drive circuit from short-circuiting to positive and negative supply voltages. The power dissipation increases when a short circuit occurs. The short-circuit protection function protects the driver stage from damage.

Over-temperature protection: TD551SCANHS has over-temperature protection. When the junction temperature exceeds 150°C, the current in the driver stage will decrease. Because the drive tube is the primary energy consuming component, current reduction can reduce power consumption and reduce chip temperature. At the same time, the rest of the chip remains functional.

Dominant time-out function: TD551SCANHS has dominant time-out function to prevent if the pin TXD is forced to a permanent low level due to a hardware or software application failure, the built-in TXD dominant timeout timer circuit prevents the bus line from being driven to a permanent dominant state (blocking all network traffic). The timer is triggered by the negative edge on pin TXD.

If the low level on pin TXD lasts longer than the internal timer value (t_{TXD_OTD}), the transmitter will be disabled and the drive bus will enter a recessive state. The timer is reset by the positive edge on pin TXD.

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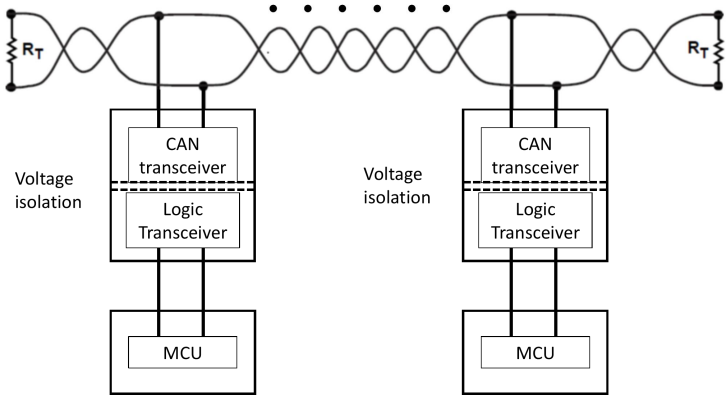


Figure 7. Typical application circuit

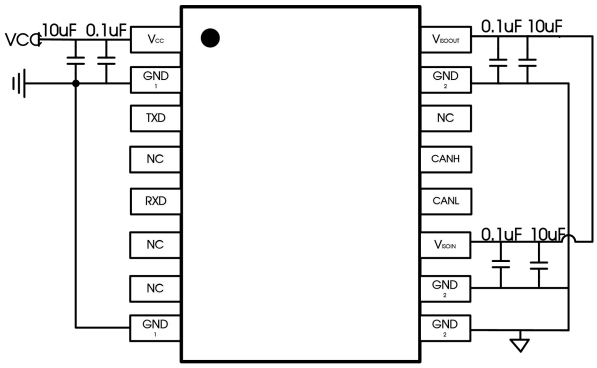
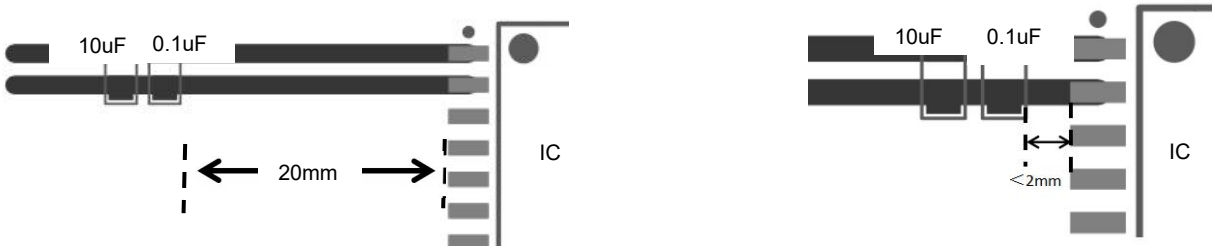


Figure 8. Typical Application of PCB layout

PCB Design Instructions

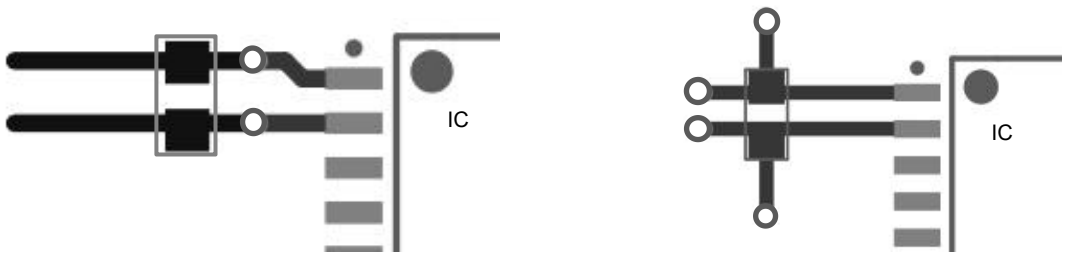
1. VCC and GND1, VISO and GND2 must be connected to 0.1uF and 10uF capacitors respectively.
2. The decoupling capacitors (0.1uF)and energy storage capacitor(10uF) of VCC and GND1, V_{ISO} and GND2 should be placed as close the chip pins as possible to the chip pins to reduce loop area and parasitic inductance of PCB traces. General control should be 2mm. The decoupling capacitor is placed close the chip, and the energy storage capacitor is placed outside. As shown in Figure 8-1.



Not Recommended　　Recommended

Figure 8-1

3. The power line width should be designed at least 0.5mm when wiring.
4. When it is necessary to place vias in the power supply line and the ground wire, the position of the vias should be placed on the outside of the capacitor relative to the chip pins, ather than between the capacitor and the chip, as shown in the figure 8-2 below to reduce the number of vias effect of parasitic inductance.



Not Recommended　　Recommended

Figure 8-2

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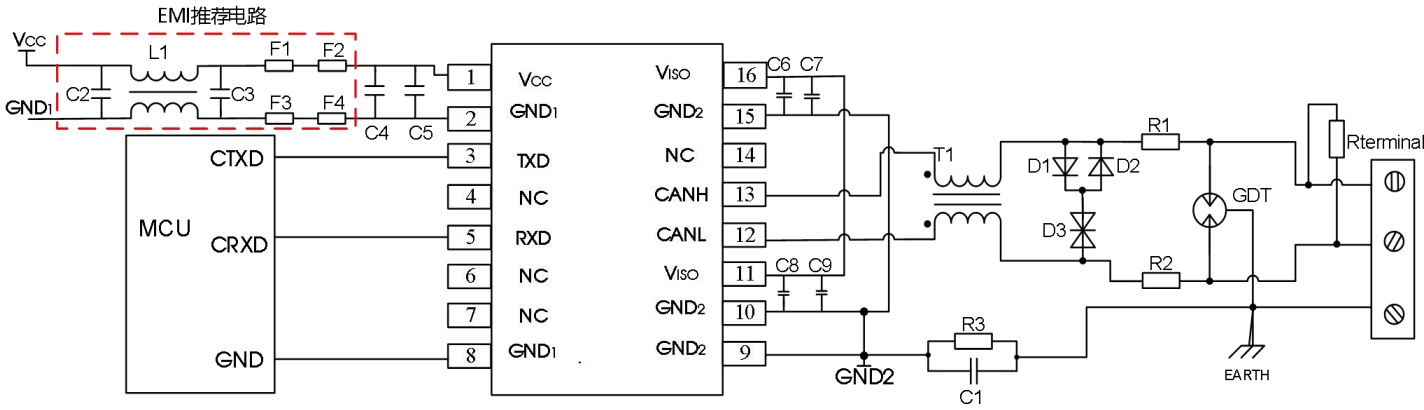


Figure 9. Port protection circuit for harsh environments

Recommend components and values:

Component	Recommend part, value	Component	Recommend part, value
R3	1MΩ	D1、D2	1N4007
C1	1nF, 2kV	D3	SMBJ30CA
T1	ACM2520-301-2P	$R_{terminal}$	120Ω
GDT	B3D090L	R1、R2	2.7Ω/2W
C2,C3,C9	10uF/16V (Surface Mount Ceramic Capacitor)	C8	0.1uF/16V (Surface Mount Ceramic Capacitor)
C4,C7 (Must Add)	10uF/16V (Surface Mount Ceramic Capacitor)	C5,C6 (Must Add)	0.1uF/16V (Surface Mount Ceramic Capacitor)
F1,F2,F3,F4	BA0805-102T	L1	FL2D-Z5-080

To improve the system's EMI performance, common-mode inductors and ferrite beads can be added at the VCC-GND front end of the module.

When the module is used in applications with harsh environment, it can be susceptible to large energy like lightning strike, etc. in which case, it is essential to add an adequate protection circuit to the CAN signal ports to protect the system from failure and maintain a reliable bus communication. Figure 9 provides a Recommend protection circuit design for high-energy lightning surges, with a degree of protection related to the selected protection device. Parameter description lists a set of Recommend circuit parameters, which can be adjusted according to the actual application situation. Also, when using the shielded cable, the reliable single-point grounding of the shield must be achieved.

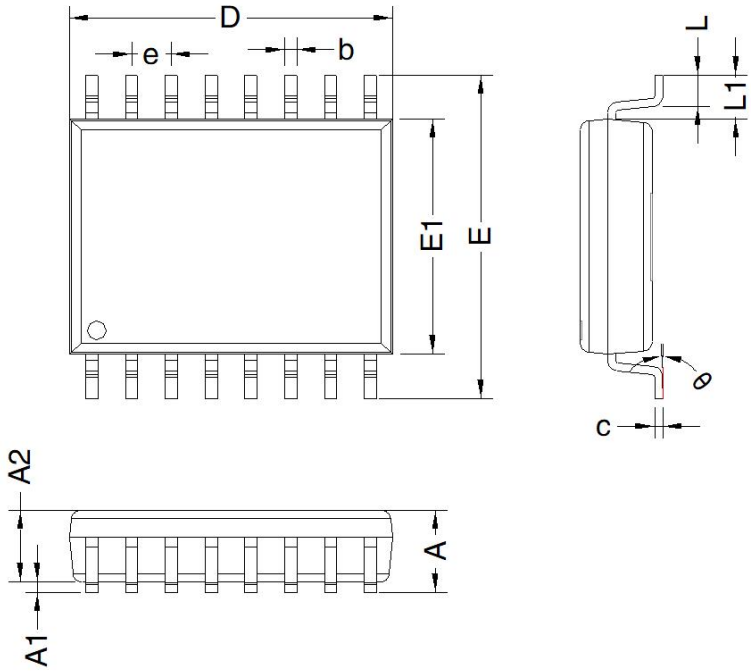
Note: The Recommend components and values is a general guideline only and must be verified for the actual user's application. We Recommend using PTC's for R1 and R2 and to use fast recovery diodes for D1 and D2.

Ordering Information

Part number	Package	Number of pins	Product marking	Tape & Reel
TD551SCANHS	SOIC	16	TD551SCANHS	340/REEL

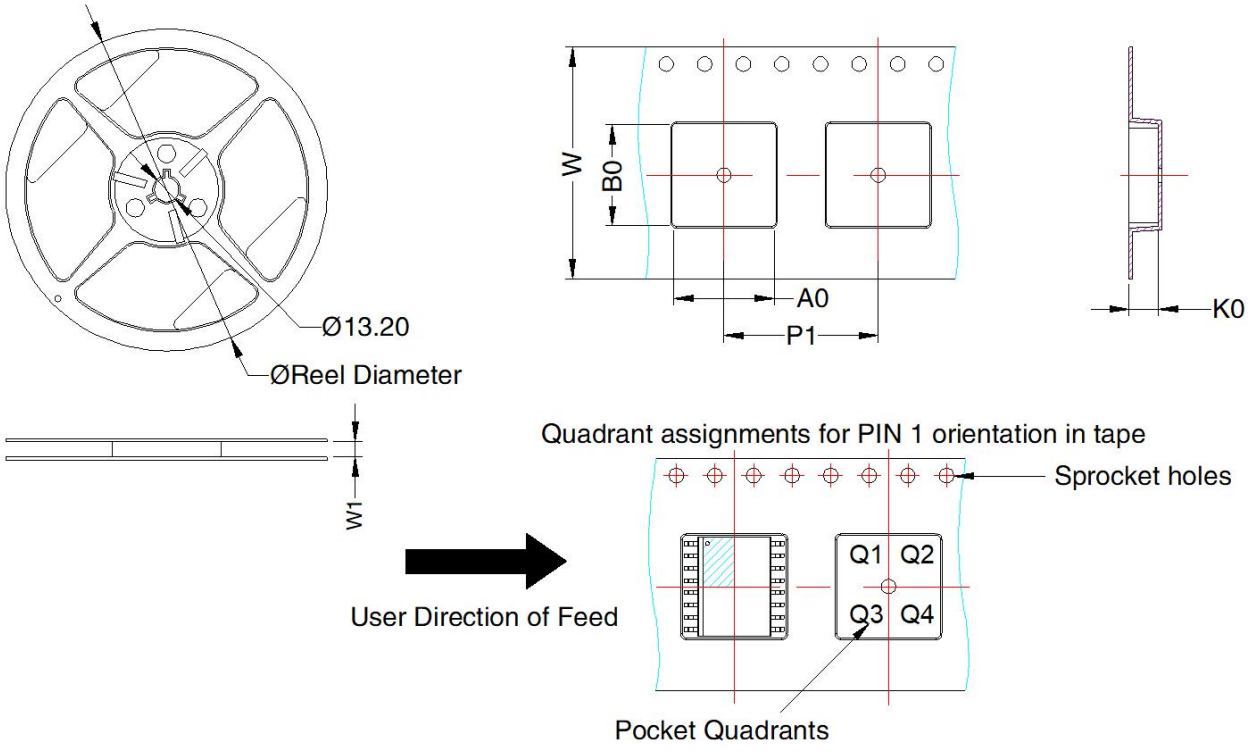
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THIRD ANGLE PROJECTION



Mark	Dimension(mm)	
	Min	Max
A	–	2.65
A1	0.10	0.30
A2	2.25	2.35
b	0.35	0.43
c	0.24	0.29
D	10.20	10.40
e	1.27 BSC	
E	10.10	10.50
E1	7.40	7.60
L	0.55	0.85
L1	1.40 BSC	
θ	0°	8°

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Package Type	Pin	MPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SOIC–16	16	340	180.0	16.4	10.74	10.65	3.05	16.0	16.0	Q1

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